

Method and system for instruction tracing with enhanced interrupt avoidance

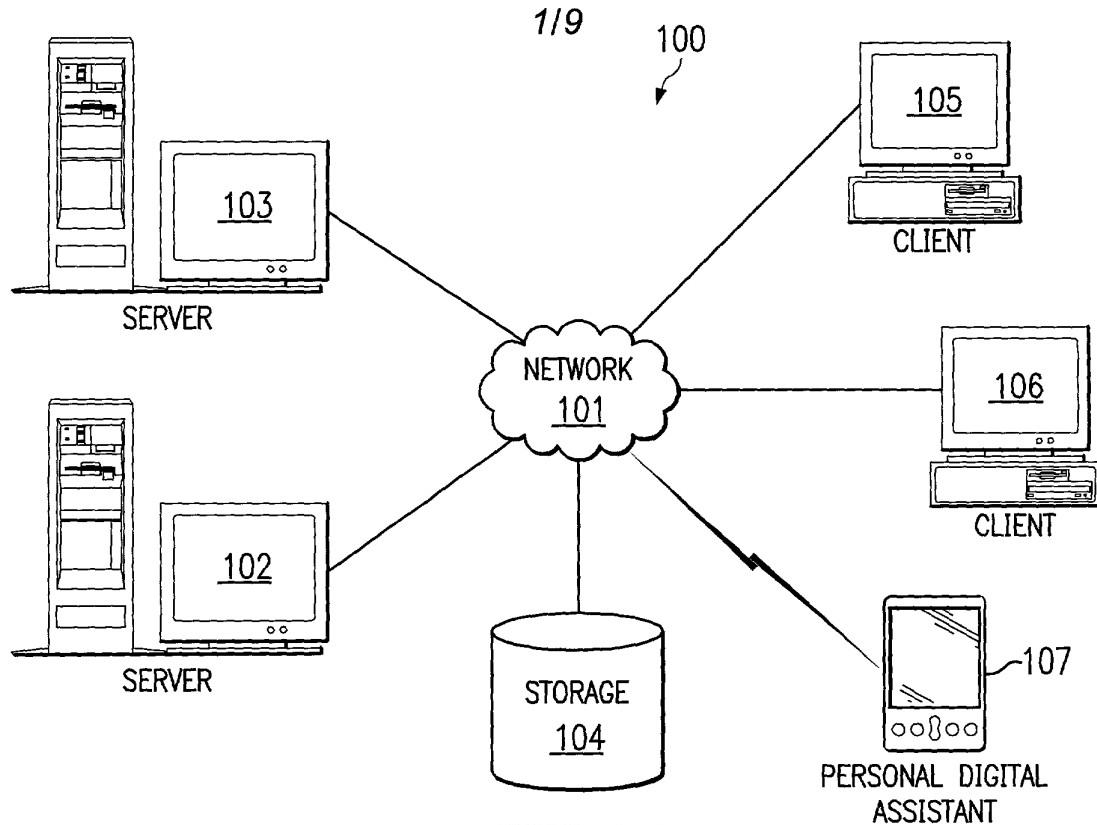


FIG. 1A
(PRIOR ART)

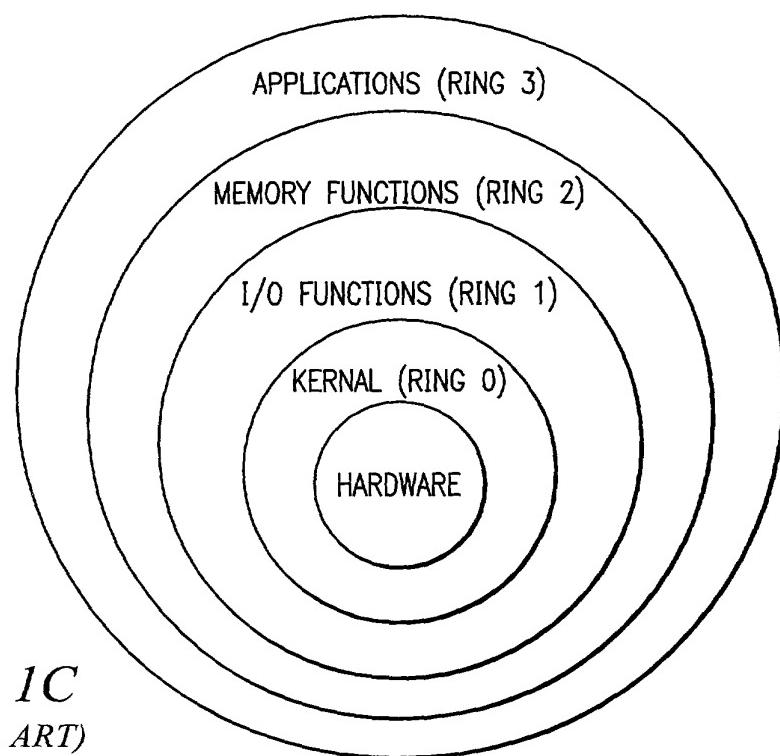
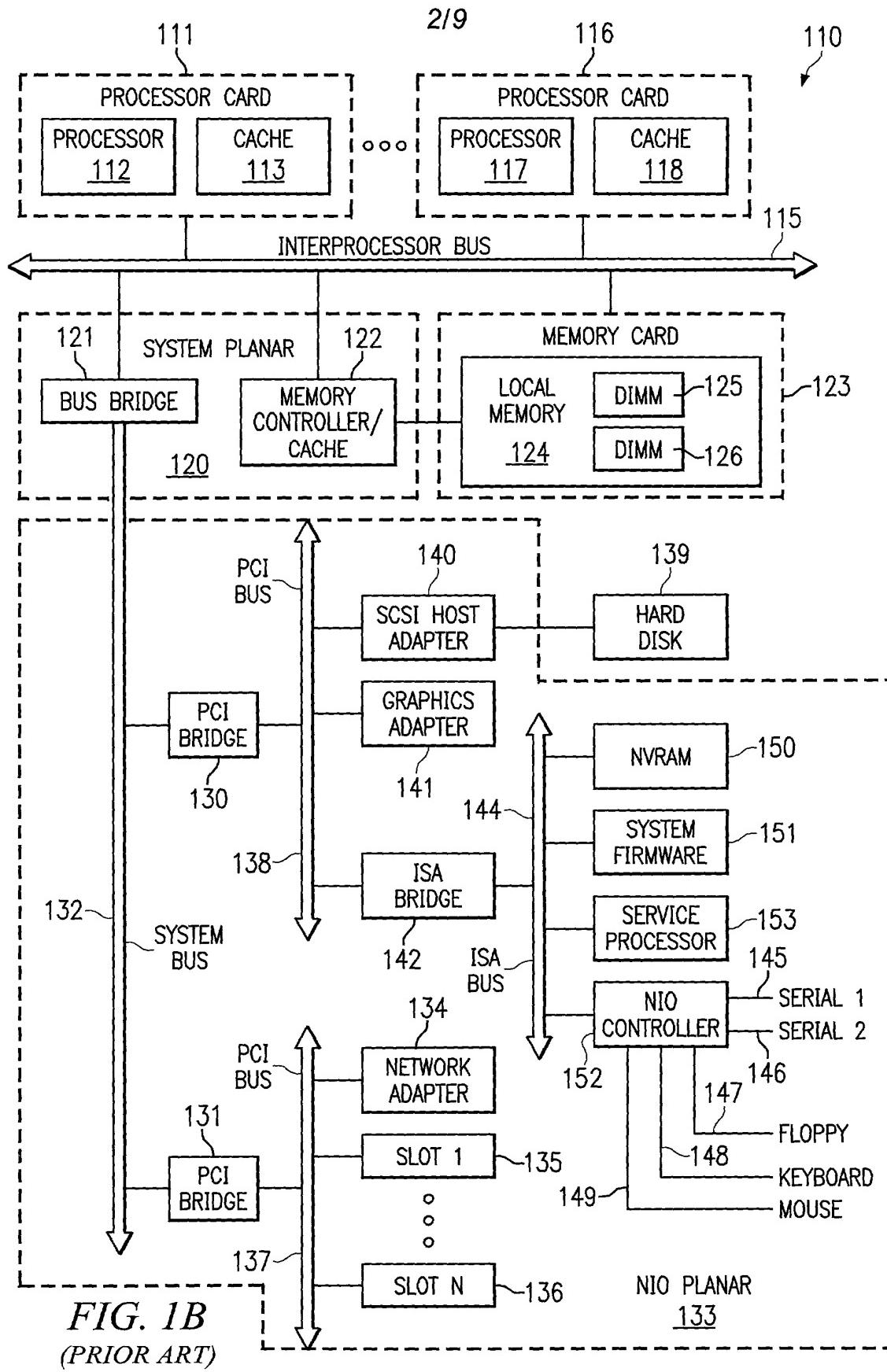


FIG. 1C
(PRIOR ART)



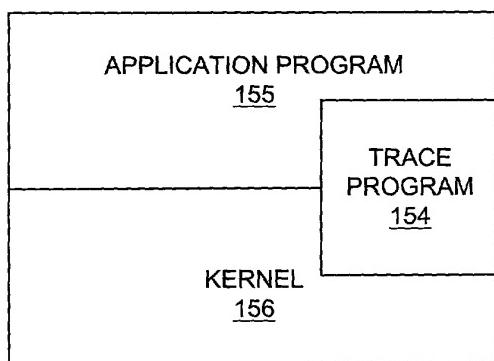


FIG. 1D
(PRIOR ART)

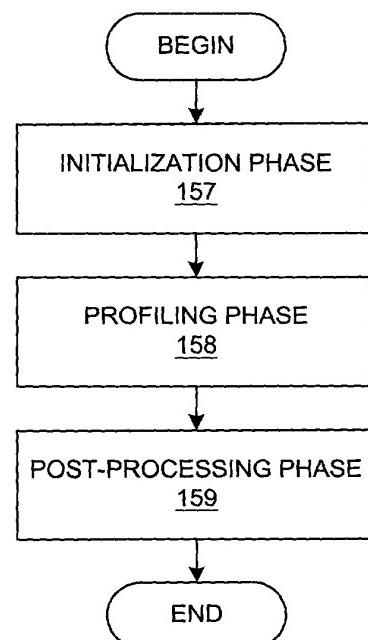


FIG. 1E
(PRIOR ART)

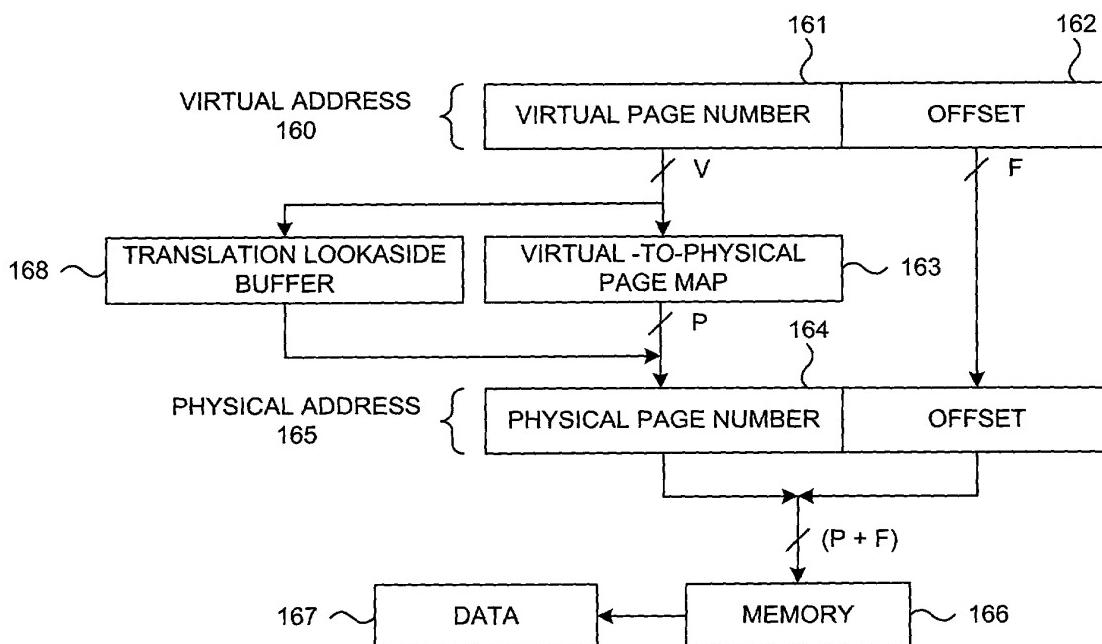


FIG. 1F
(PRIOR ART)

Method and system for instruction tracing with enhanced interrupt avoidance

4/9

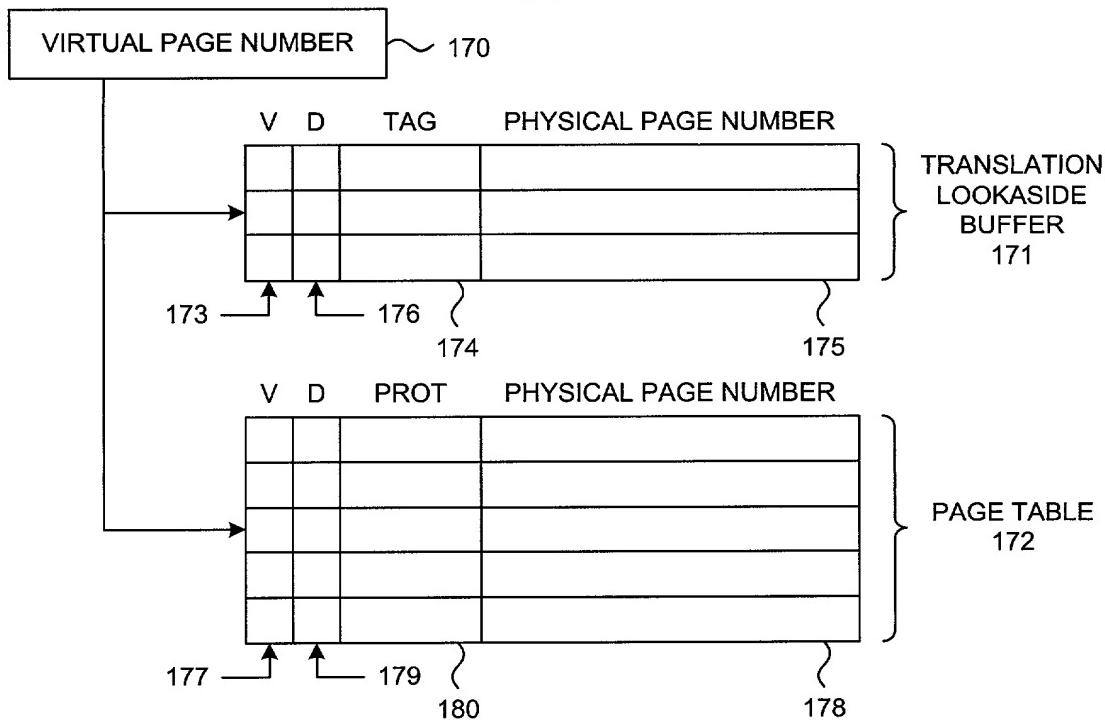


FIG. 1G
(PRIOR ART)

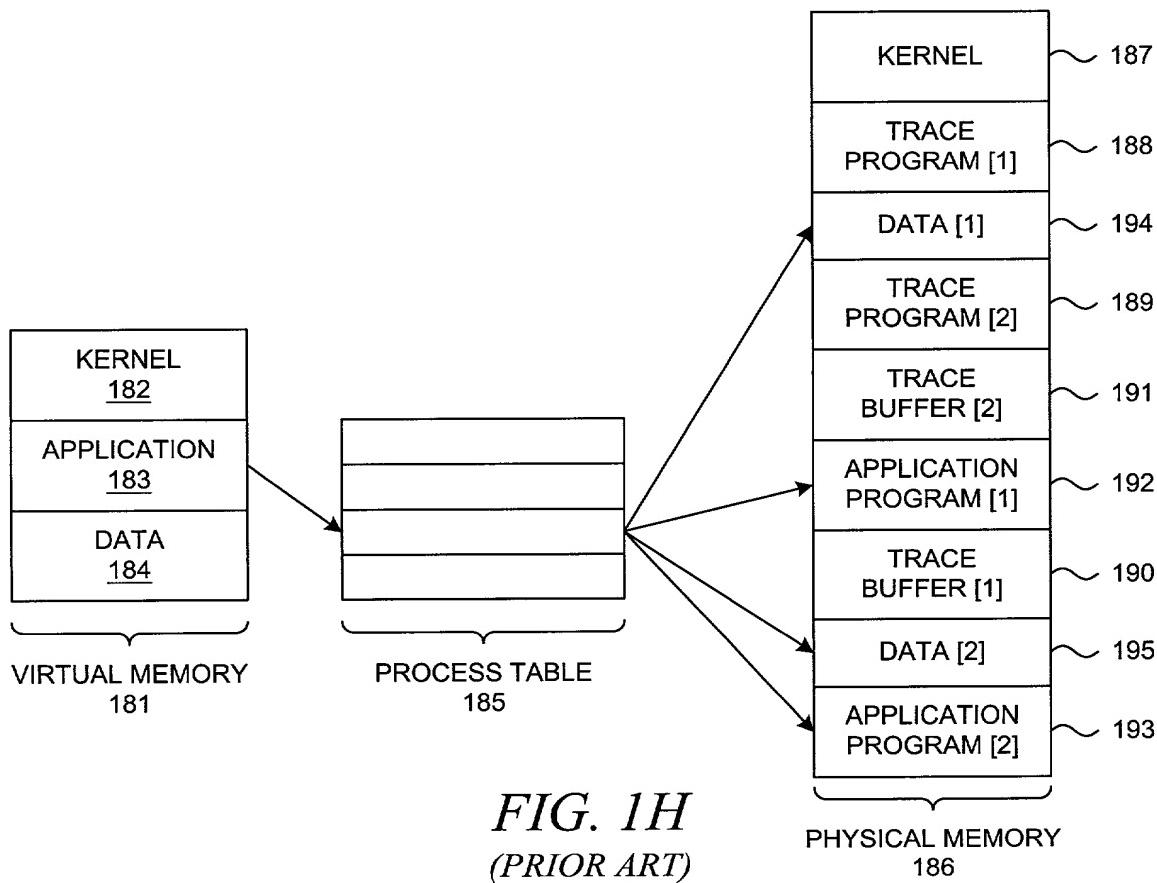
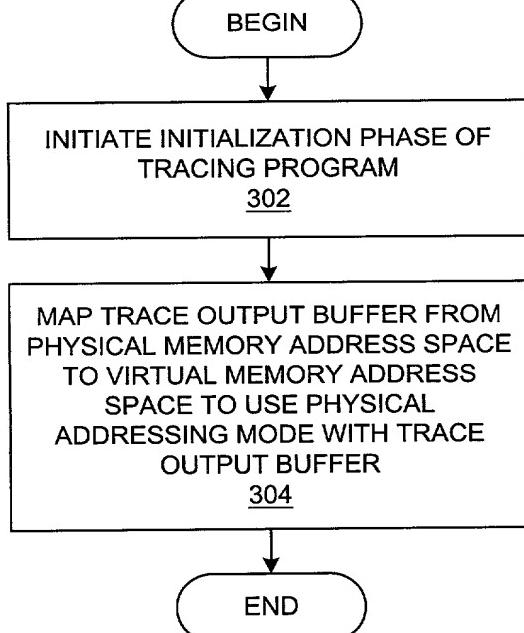
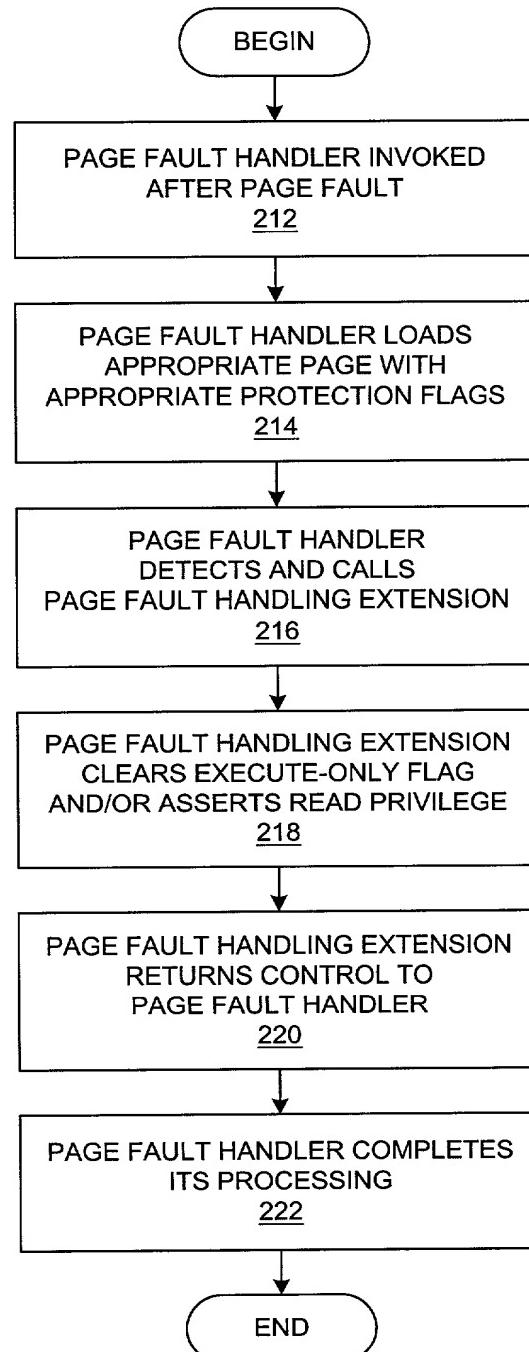
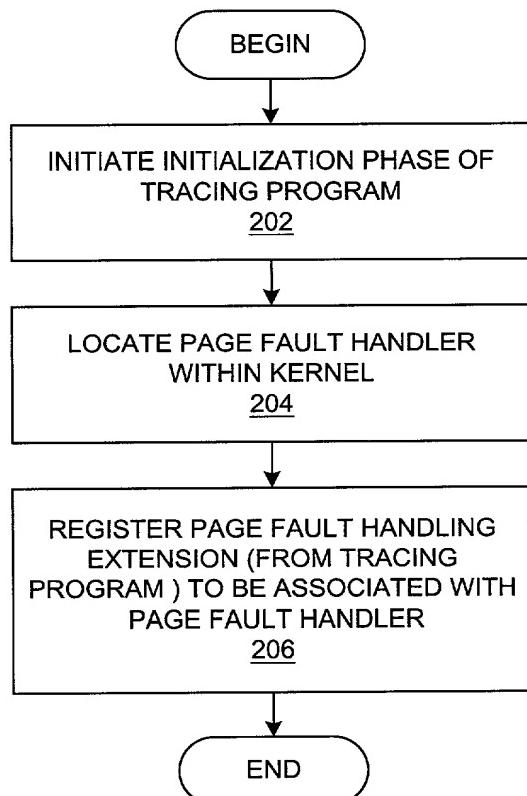
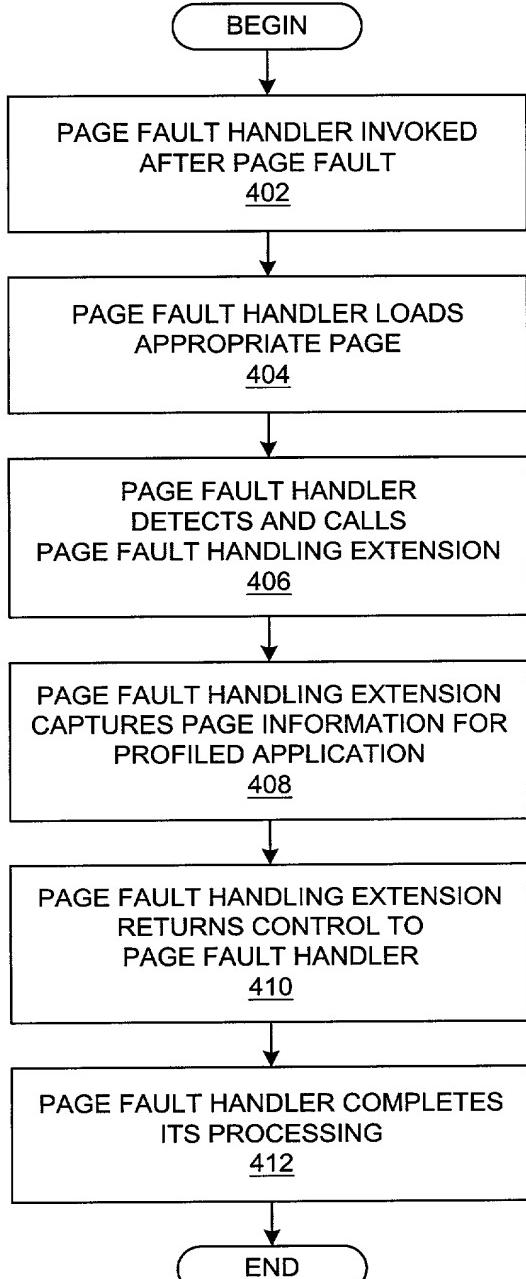
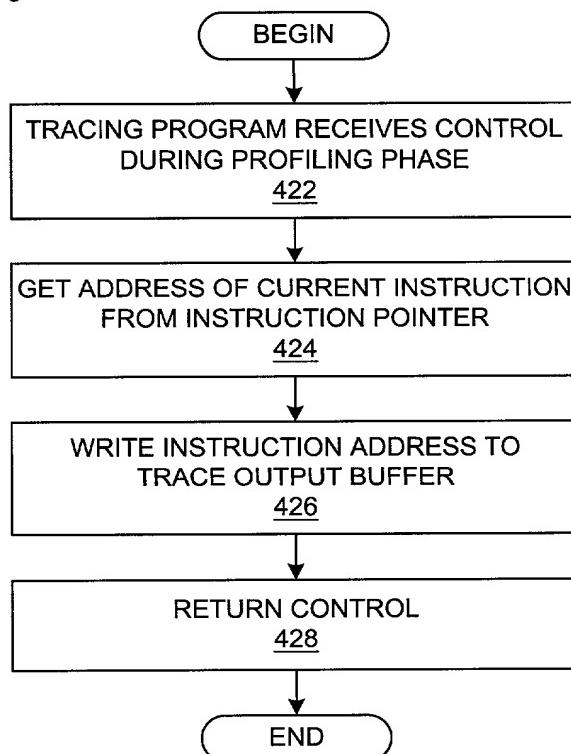
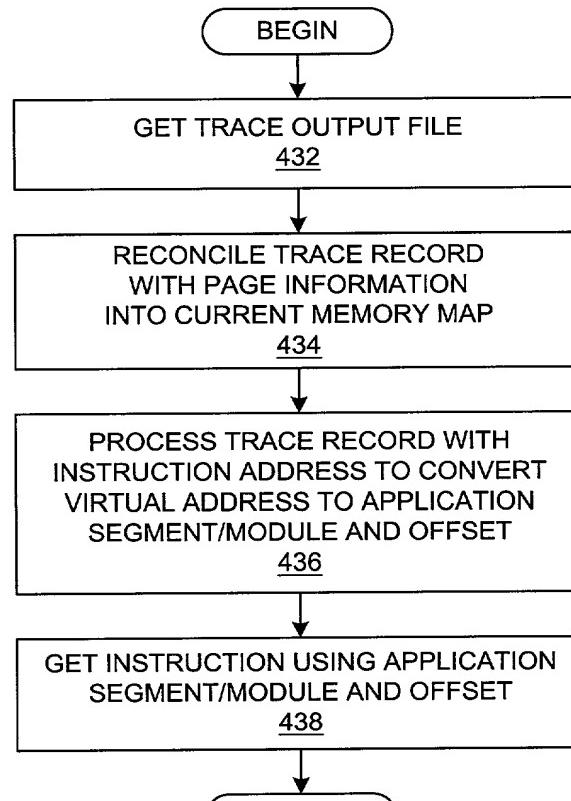


FIG. 1H
(PRIOR ART)

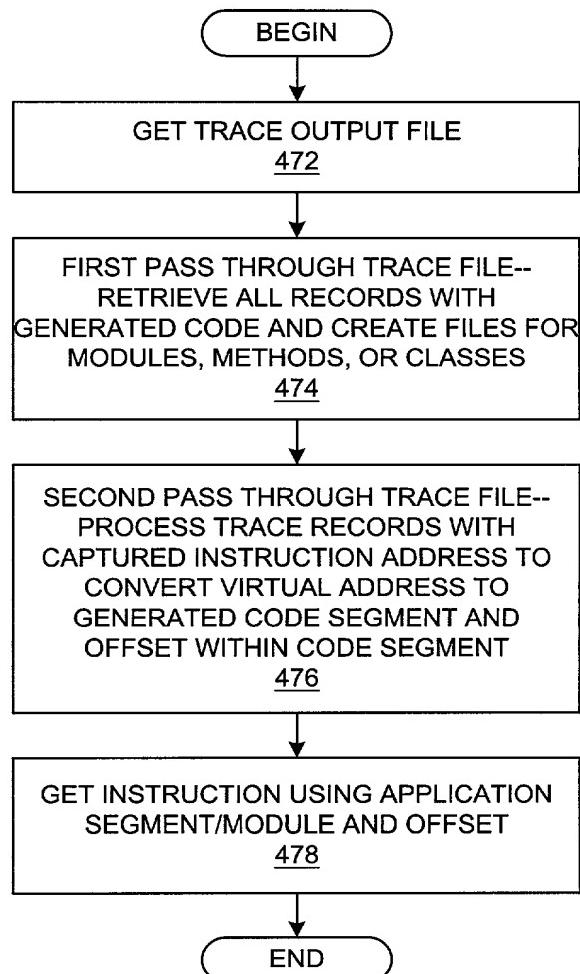
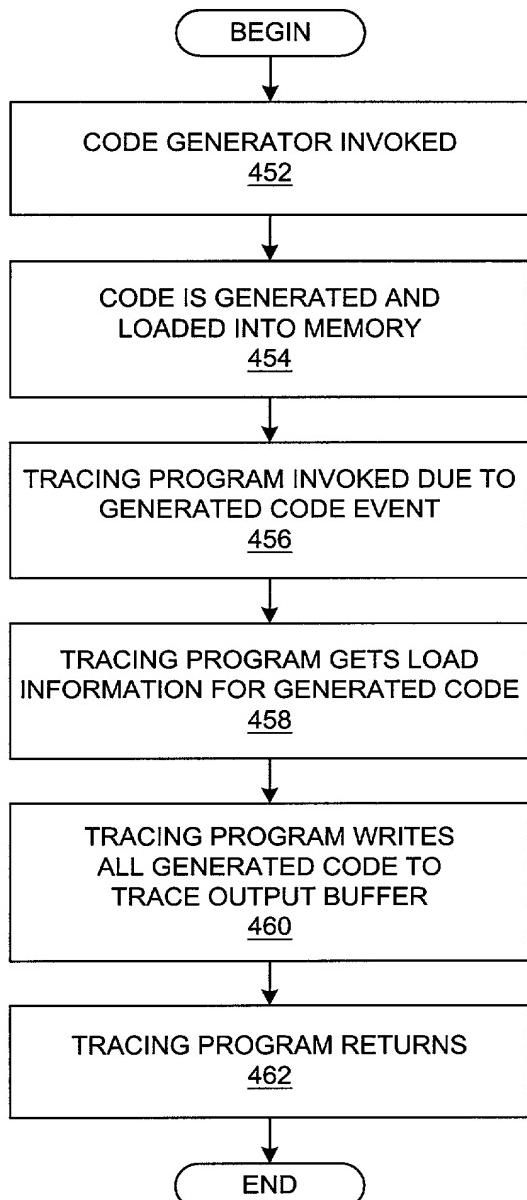
**FIG. 3**

10045307 v.01/14

6/9

*FIG. 4A**FIG. 4B**FIG. 4C*

7/9



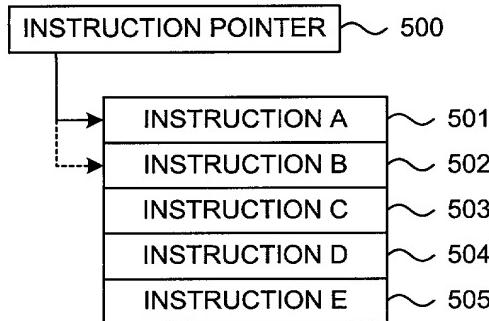


FIG. 5A

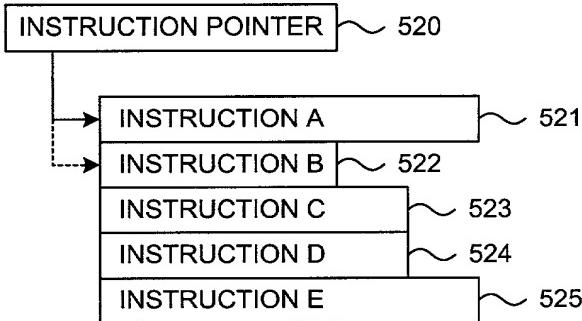


FIG. 5C

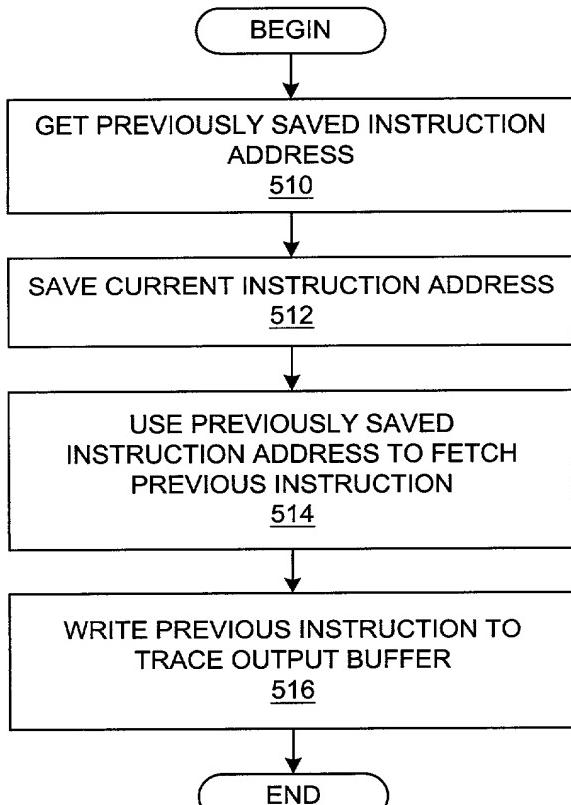


FIG. 5B

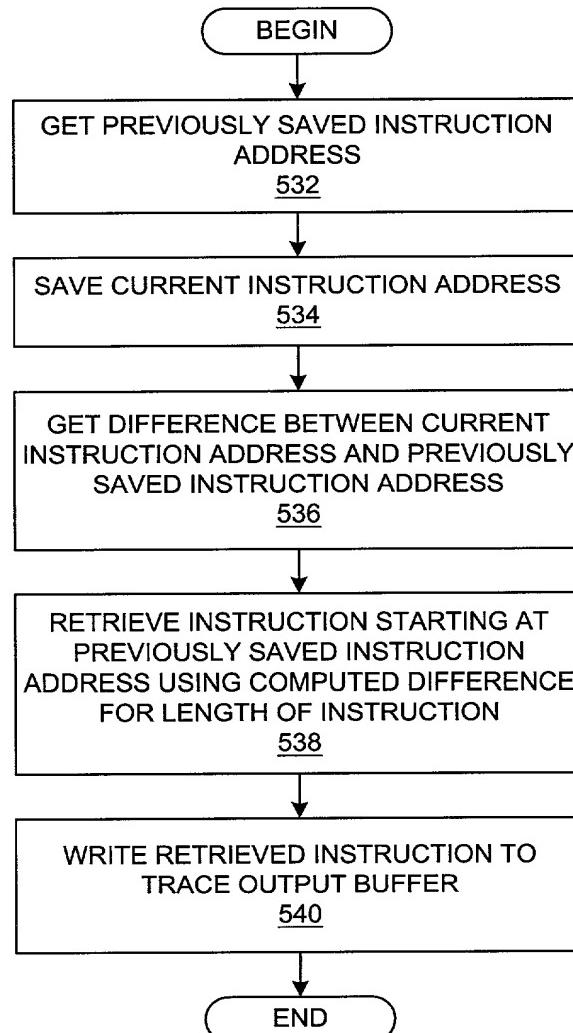
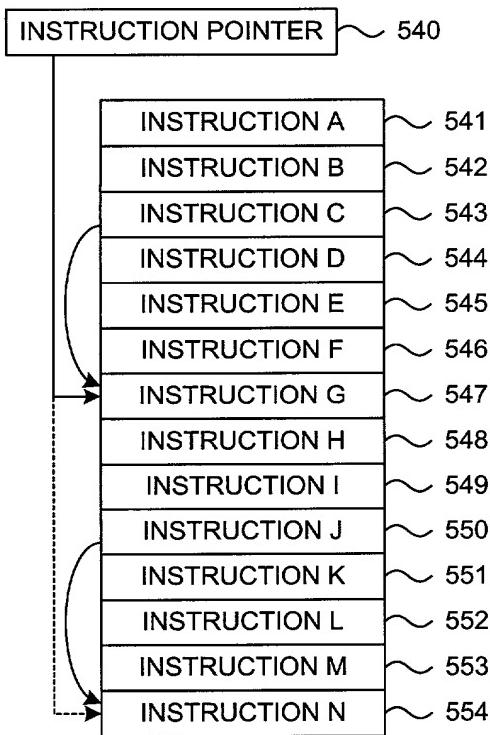
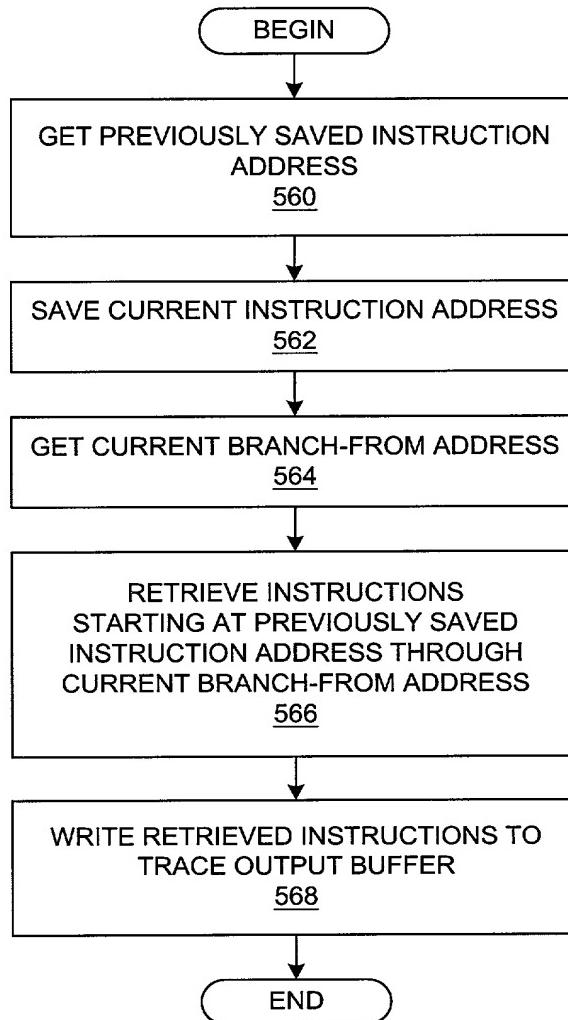


FIG. 5D

*FIG. 5E**FIG. 5F*